Lab231 & 232 (CY Lab)

Prof. Chun-Yao Wang (王俊堯)
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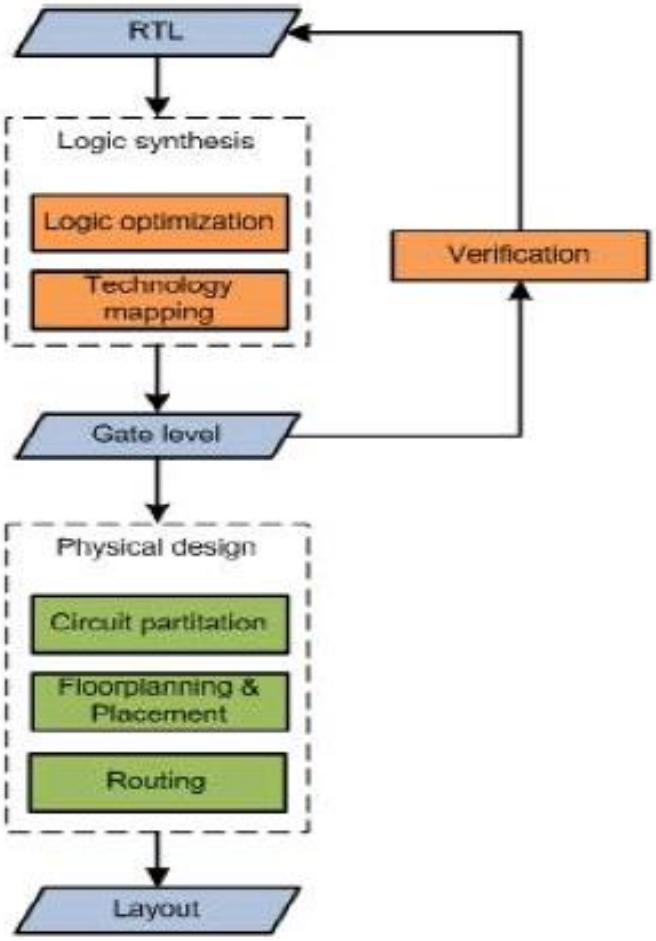
Introduction

- Established in Feb. 2003
- A part of VLSI/CAD Lab

- Office/Lab is located at
  Delta R618/CL(炯朗館) R231&R232
- Website: http://nthucad.cs.nthu.edu.tw/~wcyao/

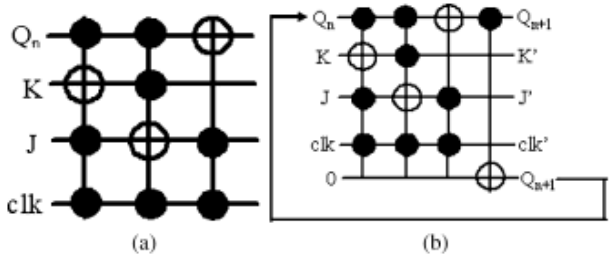
Research Interests (1/2)

- VLSI design automation
  - Verification
  - Logic synthesis
- Hardware security
- EDA for AI model reduction

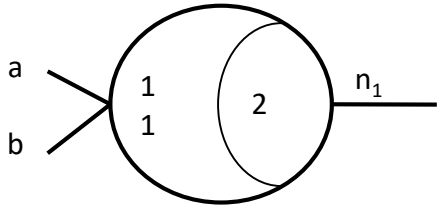


Research Interests (2/2)

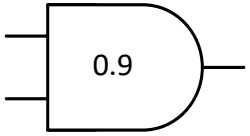
- Emerging technologies (Quantum circuits, Single Electron Transistor circuits, Memristor circuits, Probabilistic CMOS)
  - Logic synthesis
    - Reversible logic



    - Threshold logic



    - Probabilistic logic

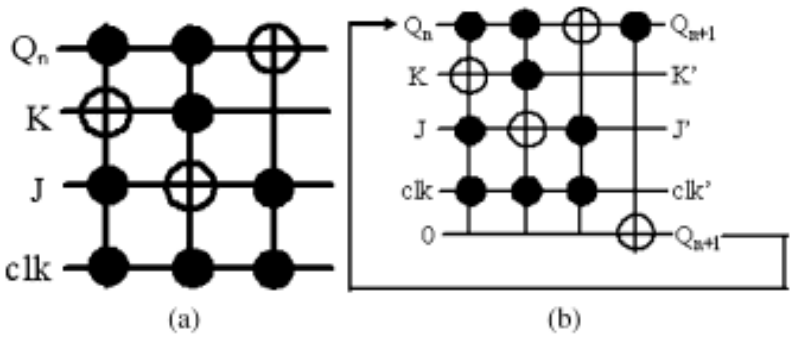


Members

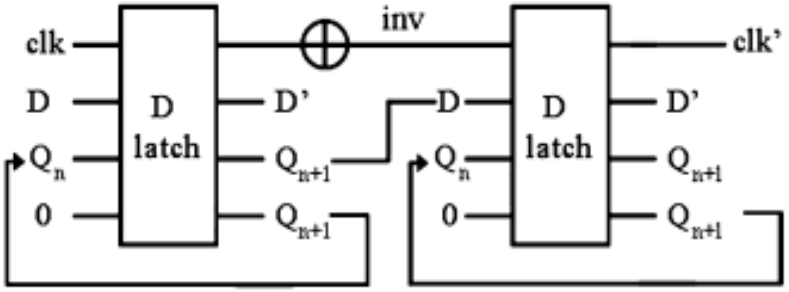
- **Graduate - Ph.D. (2)**
  - 李奕霆 唐梧遷
- **Graduate - M.S. (12)**
  - (113) 白琪澤 許明騏 程采婕 王柏穎 黃霈紳
  - (114)黃守翊 沈安婕 蔡皓宇 王子銜 林哲健 邱珮綸 洪梓翔

Selected Research Results

- **Synthesis**
  - "Synthesis of Reversible Sequential Elements" (ACM JETC 2008)

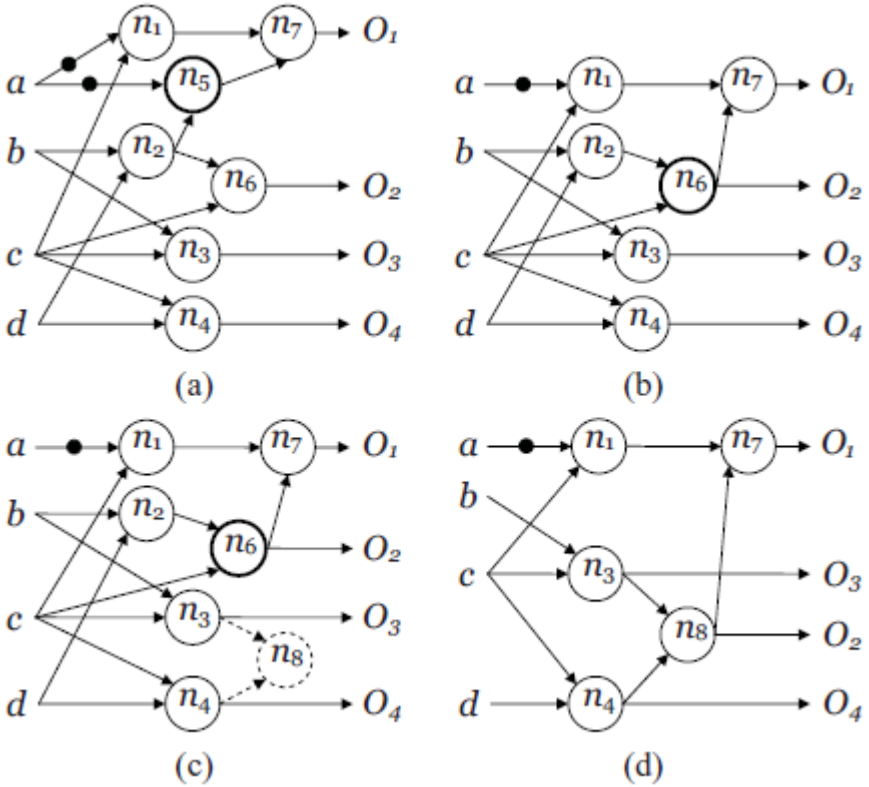


Reversible JK latch



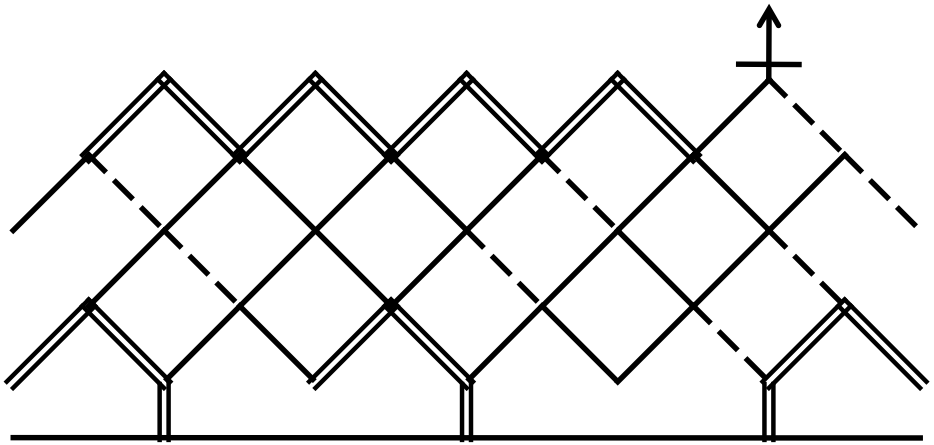
Reversible D flip-flop

- **Synthesis**
  - "Node Addition and Removal in the Presence of Don't Cares" (DAC 2010, Best Paper Nominee, IEEE TCAD 2012)

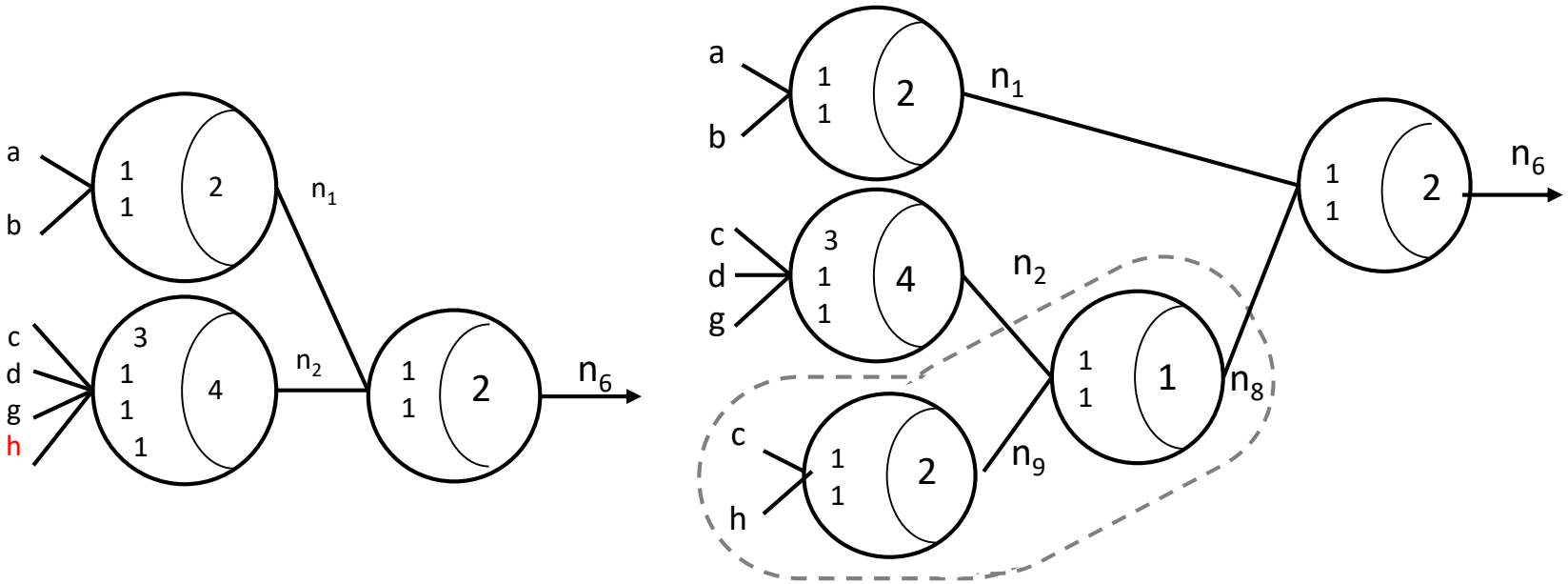


"Fast Node Merging with Don't Cares Using Logic Implications" (ICCAD 2009, IEEE TCAD 2010)

- **Synthesis**
  - "Automated Mapping for Reconfigurable Single-Electron Transistor Arrays" (DAC 2011, ACM JETC 2012)
  - "Width Minimization in the Single-Electron Transistor Array Synthesis" (DATE 2014, IEEE TVLSI 2015)
  - "BDD-Based Synthesis of Reconfigurable Single-Electron Transistor Arrays" (ICCAD 2014)
  - "Dynamic Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays" (IEEE TVLSI 2017)
  - "Diagnosis for Reconfigurable Single-Electron Transistor Arrays with a More Generalized Defect Model" (ACM JETC 2021)

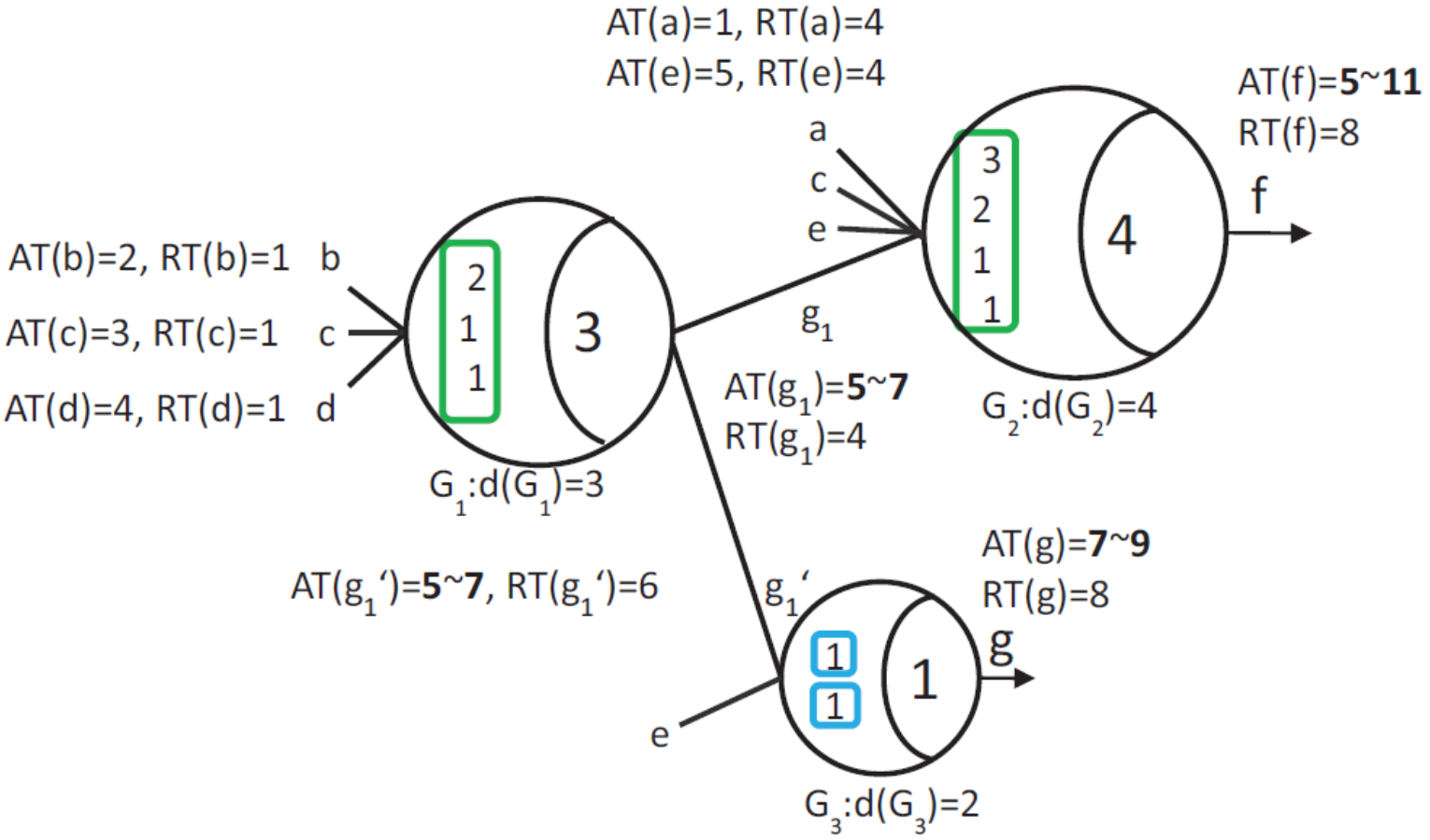


- **Synthesis**
  - "On Rewiring and Simplification for Canonicity in Threshold Logic Circuits" (ICCAD 2011)

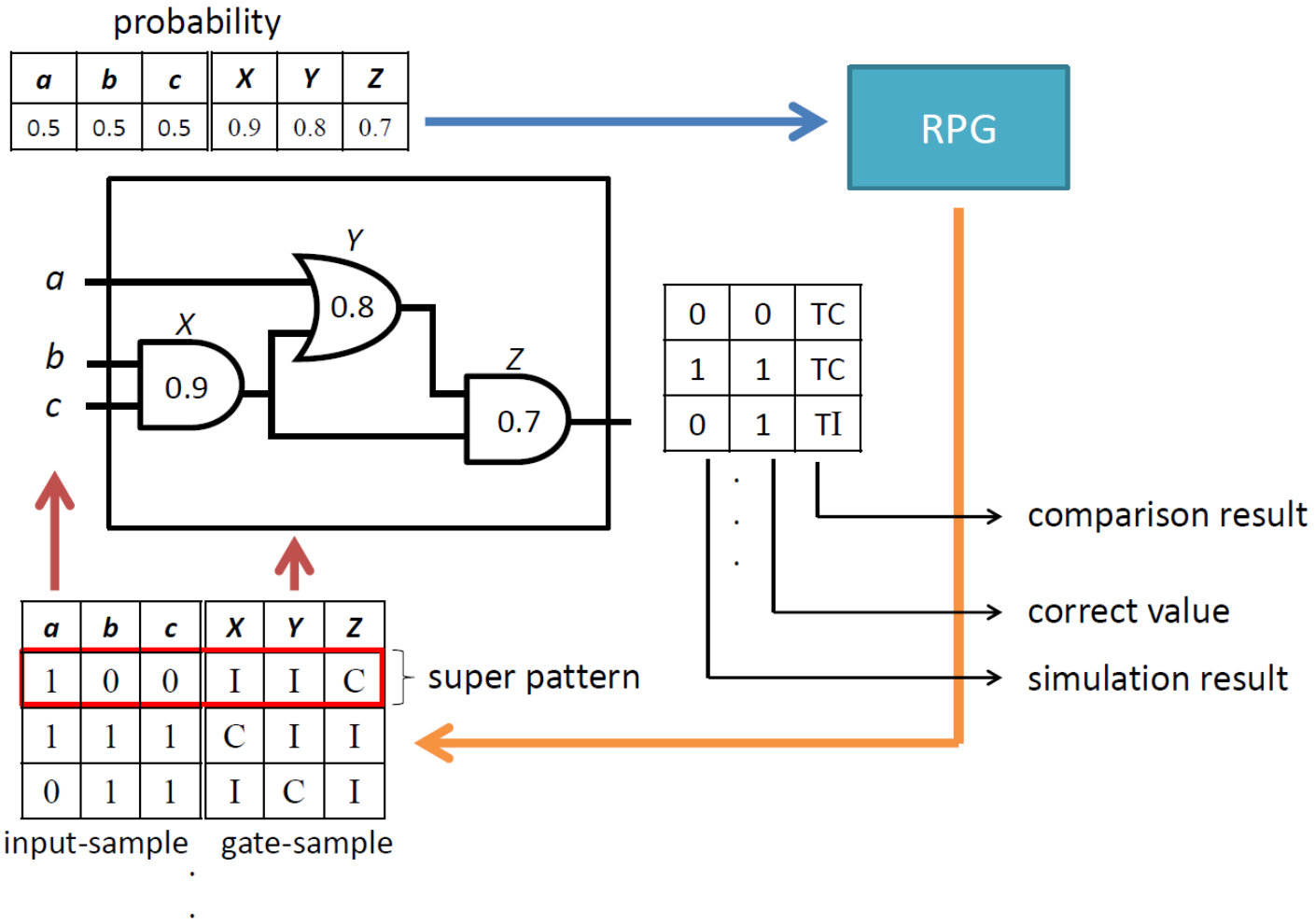


The rectification network for h's removal

- **Synthesis**
  - "Sensitization Criterion for Threshold Logic Circuits and its Application" (ICCAD 2013)

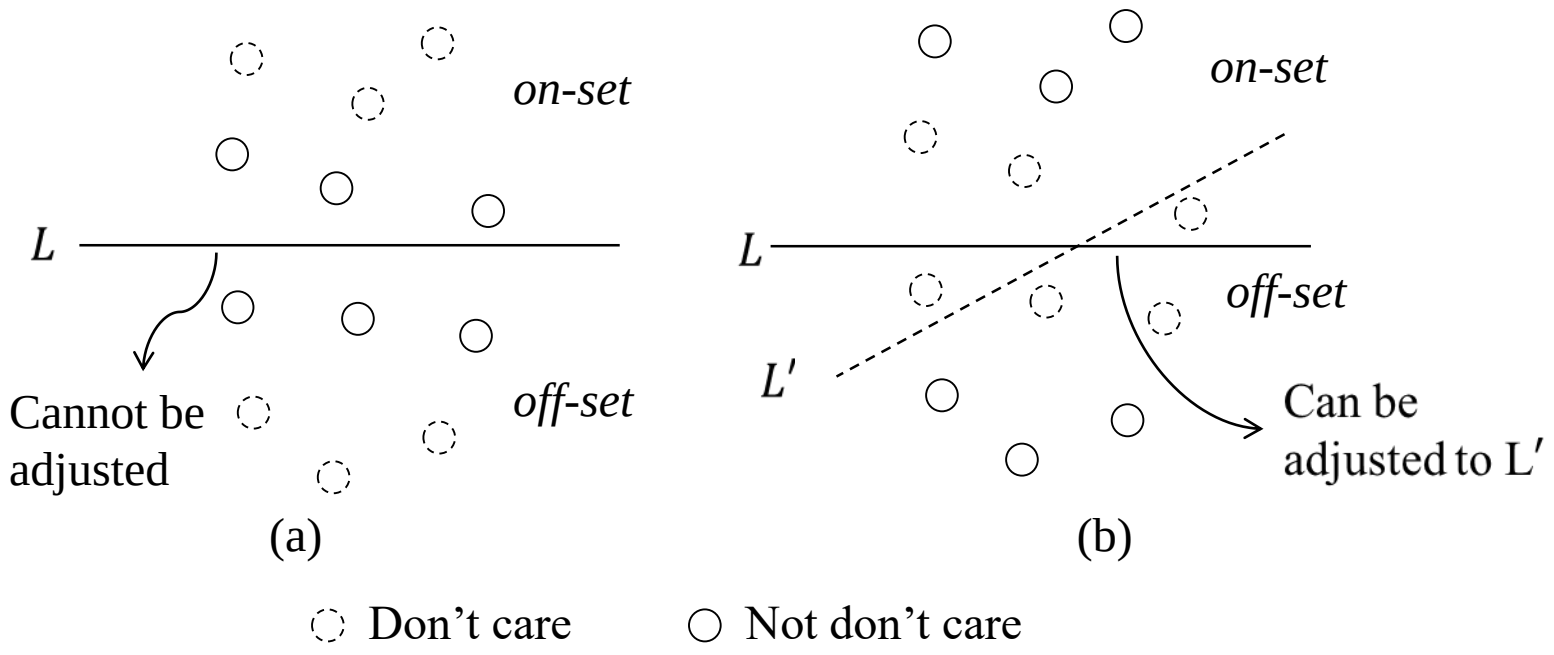


- **Synthesis**
  - "Correctness Analysis and Power Optimization for Probabilistic Boolean Circuits"(IEEE TCAD 2015)

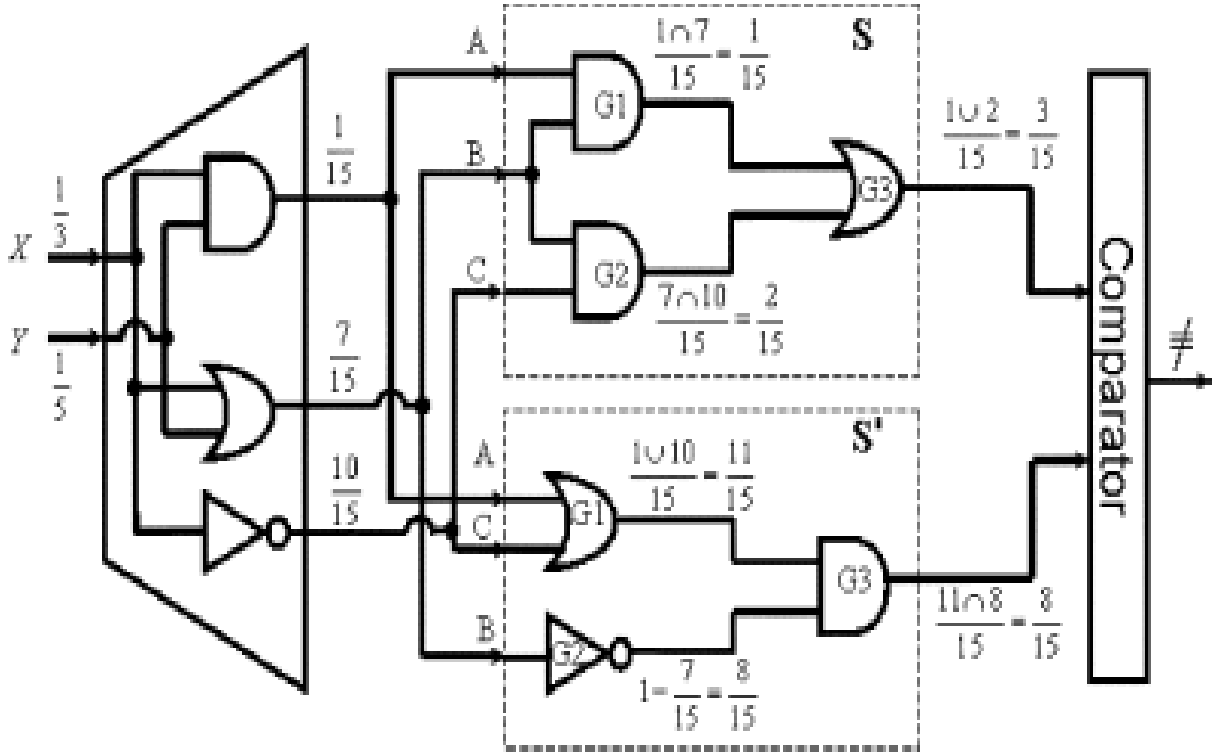


- **Synthesis**
  - "On Synthesizing Memristor-Based Logic Circuits with Minimal Operational Pulses"(IEEE TVLSI 2018)
  - "Threshold Function Identification by Redundancy Removal and Comprehensive Weight Assignments" (IEEE TCAD 2019)
  - "A New Necessary Condition for Threshold Function Identification" (IEEE TCAD 2020)
  - "Don't Care Computation and De Morgan Transformation for Threshold Logic Network Optimization" (IEEE TCAD 2022)

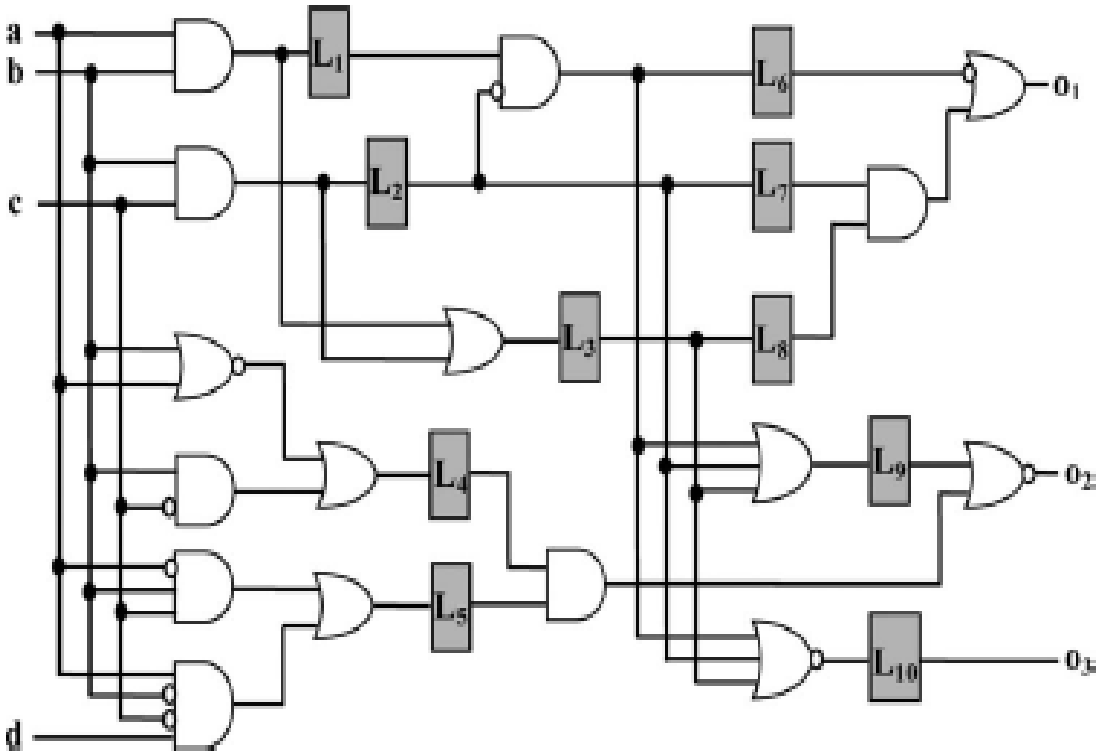
- **Synthesis**
  - "A Constructive Approach for Threshold Function Identification" (ACM TODAES 2023)
  - "9-input Threshold Function Identification using a New Necessary Condition of Threshold Function" (IEEE TCAD 2024)



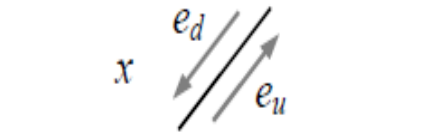
- **Verification**
  - "Novel Probabilistic Combinational Equivalence Checking" (IEEE TVLSI 2008)



- **Verification**
  - "Dependent Latch Identification in Reachable State Space" (ASPDAC 2009, Best Paper Nominee, IEEE TCAD 2009)

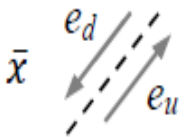


- **Verification**
  - "Verification of Reconfigurable Binary Decision Diagram-based Single-Electron Transistor Arrays" (IEEE TCAD 2013)



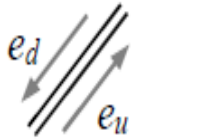
$(\neg x \vee e_u \vee e_d) \wedge (\neg x \vee \neg e_u \vee \neg e_d) \wedge (x \vee \neg e_u) \wedge (x \vee \neg e_d)$

(a) Active high



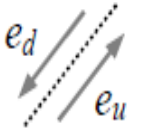
$(x \vee e_u \vee e_d) \wedge (x \vee \neg e_u \vee \neg e_d) \wedge (\neg x \vee \neg e_u) \wedge (\neg x \vee \neg e_d)$

(b) Active low



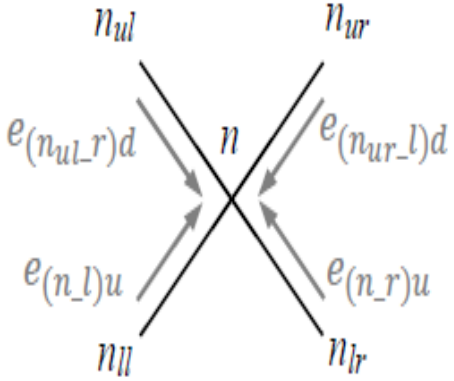
$(e_u \vee e_d) \wedge (\neg e_u \vee \neg e_d)$

(c) Short



$(\neg e_u) \wedge (\neg e_d)$

(d) Open



(a)

$$n = n_{ul}e_{(n_{ul}\_r)d} + n_{ur}e_{(n_{ur}\_l)d} + n_{ll}e_{(n\_l)u} + n_{lr}e_{(n\_r)u}$$

(b)

- **Hardware Security**
  - “LOOPLock : LOgic OPtimization based Cyclic Logic Locking” (IEEE TCAD 2020)
  - “LOOPLock 2.0 : An Enhanced Cyclic Logic Locking Approach” (IEEE TCAD 2021)
  - “An Approach to Unlocking Cyclic Logic Locking - LOOPLock 2.0” (ICCAD 2022)
  - “LOOPLock 3.0 : A Robust Cyclic Logic Locking Approach” (ASPDAC 2024)

Publications (2008~ Present)

- Top journal papers
  - IEEE Trans. CAD *14
  - IEEE Trans. VLSI *5
  - ACM TODAES *2
  - ACM J. Emerging Technology of Computing *3
- Top conference papers
  - DAC *3
  - ICCAD *8
  - DATE *11
  - ASPDAC *9

Honors

2008	清華大學 校傑出教學獎
2008	CAD Contest 定題組 特優
2009	中國電機工程學會 優秀青年電機工程師獎
2011	國科會 優秀年輕學者研究計劃
2013	清華大學 校傑出教學獎
2013	台灣積體電路設計學會 傑出年輕學者獎
2013	CAD Contest@ICCAD 亞軍
2015	DATE最佳海報論文提名
2016	清華大學 教師榮譽教學獎
2016	清華大學 特聘教授
2016	CAD Contest@ICCAD 亞軍

2018	清華大學 傑出導師獎
2018	CAD Contest@ICCAD 冠軍
2018	VLSI-DAT 最佳論文獎
2018	CAD Contest@ICCAD 亞軍
2019	CAD Contest@ICCAD 亞軍、季軍
2020	中國電機工程學會 傑出電機工程教授獎
2022	中國電機工程學會 青年論文獎 第二名、第三名指導獎
2022	教育部優良教師
2023	清華大學電資學院 實作專題競賽 金牌
2023	教育部師鐸獎
2024	中華民國資訊學會 李國鼎磐石獎
2024	中華民國資訊月 傑出資訊人才獎
2024	CAD Contest@ICCAD 冠軍、亞軍、季軍

Photos 2004

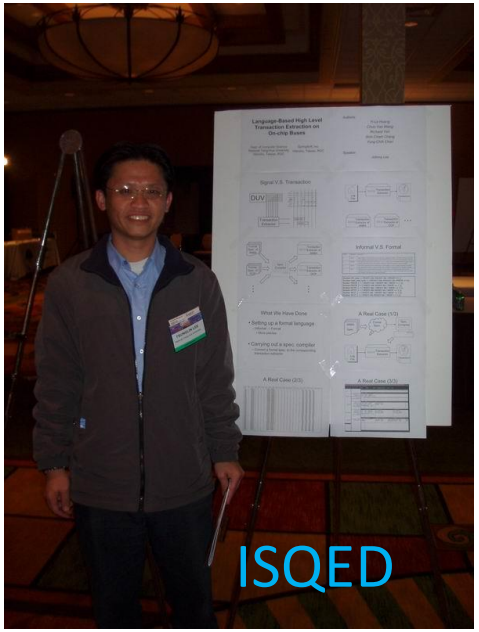
Photos 2005

小貝首次現身

DAC

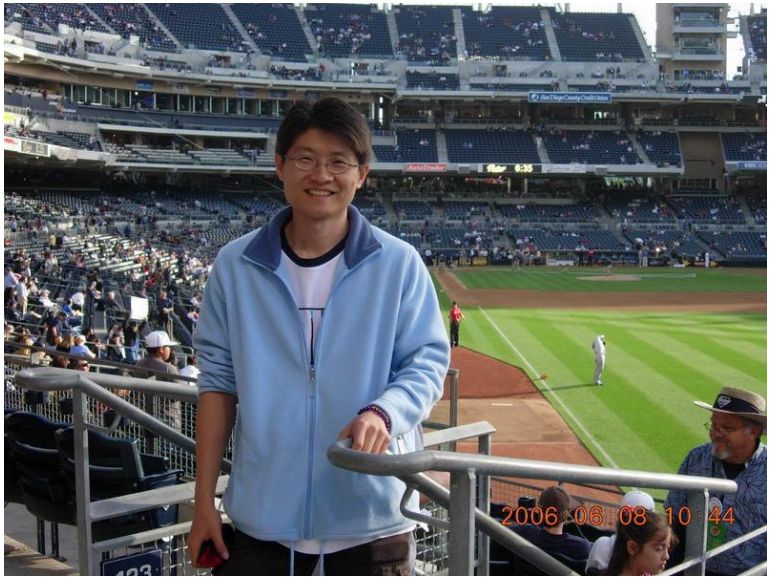
ICCD

Photos 2006



Photos 2007

ASPDAC



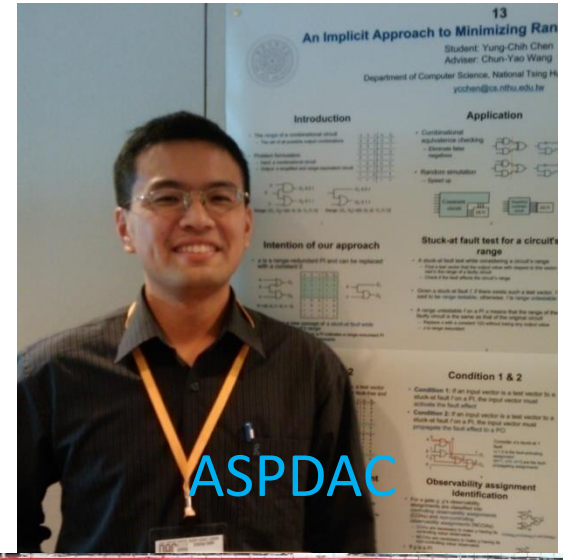
IWLS & DAC

Photos 2008

PENTAX Optio S6 F2.7 1/160s ISO100

2008-06-15 碩士

Photos 2009

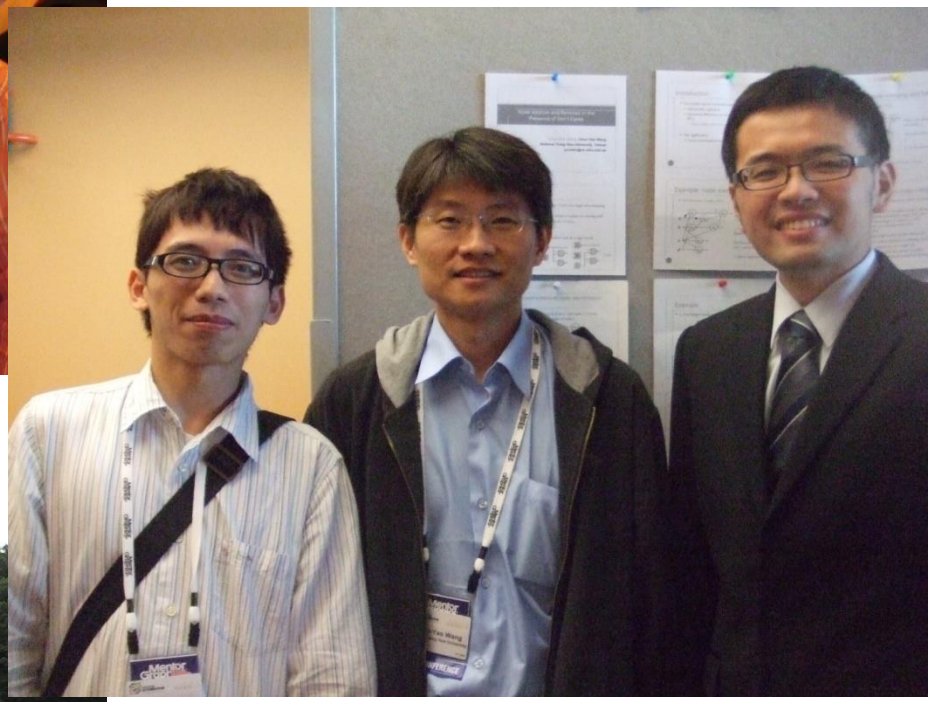


ASPDAC

勇志學長女兒出生了

Photos 2010

DAC

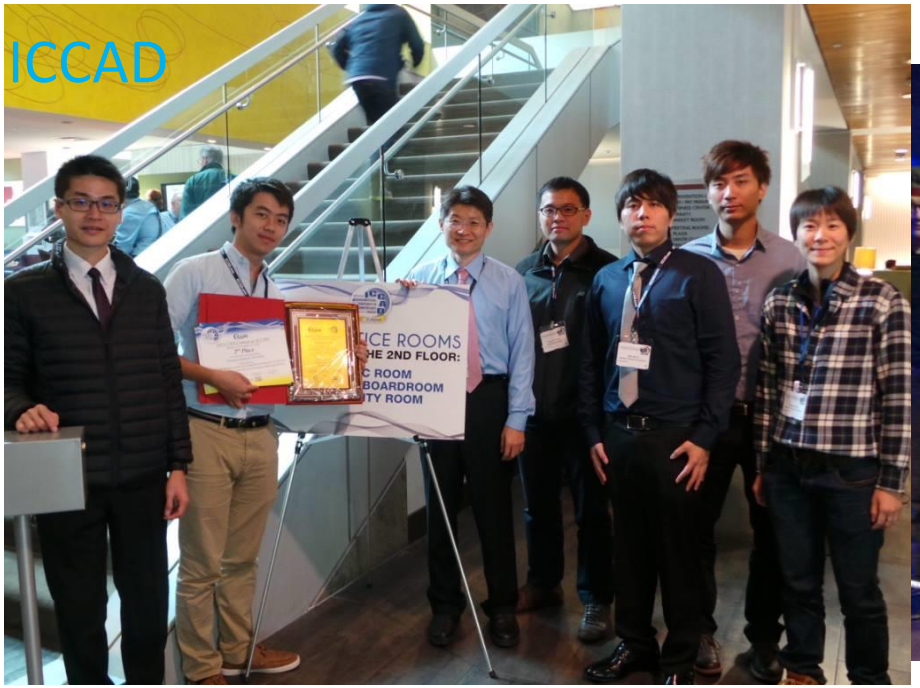


Photos 2011

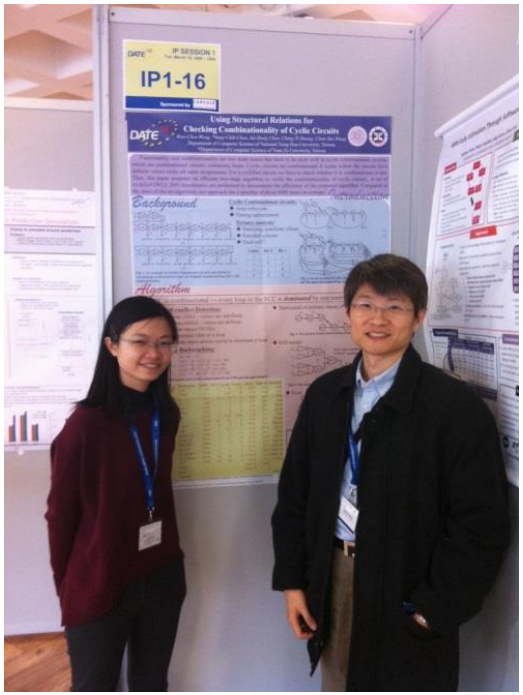
Photos 2012

Photos 2013

Photos 2014



Photos 2015


IP1-16
Using Structural Relations for
Checking Combinationality of Cyclic Circuits
Background
Algorithm

Photos 2016

三次傑出教學獎

Photos 2017

大家快看~

Photos 2018

傑出導師獎

CAD Contest 冠軍

Photos 2019

VLSI-DAT Best Paper Award

Photos 2020

傑出電機工程教授獎

Photos 2021


我原是愛聽蛩聲與鐸聲的 今卻為你感戚於小院的陰晴
算了吧 管他一世的緣份是否相值於千年慧根
誰讓你我相逢 且相逢於這小小的
鄭愁予〈錯〉
鄭愁予〈水巷〉


I NTHU

Photos 2022

教育部優良教師獎

Photos 2023

師鐸獎

Photos 2024

傑出資訊人才獎

Photos 2025

李國鼎穿石獎

傑出導師獎

Research Projects

- 透過整合設計與檢測自動化技術全面提升SoC的可靠性與安全性之研究-子計畫一：硬體木馬檢測、診斷與移除~2028/07 (NSTC)
- 拳智拳能：智慧拳擊場館建置與精準訓練系統研發—拳智拳能：智慧拳擊場館建置與精準訓練系統研發 ~2026/12 (NSTC)
- 應用於XR之Multi-model Multi-device AI軟硬體架構探索及優化的研究 ~2026/04 (NSTC)
- 以向量模擬方式來進行之量子電路的等價性驗證及錯誤診斷之研究~2027/07 (NSTC)

Recent Research Topics

- Emerging Technology
  - DIG Synthesis
- Logic Synthesis
  - Linear threshold logic circuit optimization
  - Approximate computing
- Hardware Security
- Heterogeneous Integration
- IR drop Analysis
- Optimization on Edge AI Model
- Automatic Prompt Engineering